

A METHOD, APPARATUS AND CIRCUIT FOR LATCHUP SUPPRESSION IN A GATE-ARRAY ASIC ENVIRONMENT

Abstract

An integrated circuit having a substrate (10), a power rail (18, 20), a sea of gates (12), and a latchup control isolation network electrically coupled to substrate (10). The latchup control isolation network electrically isolates sea of gates (12) from power rail (18, 20). In another embodiment, an active clamp network may be utilized to electrically isolate sea of gates (12) from power rail (18, 20). Substrate (10) includes a voltage potential. When the voltage potential is equal to or greater than a first predetermined value or the voltage potential is equal to or less than a second predetermined value, either the latchup control isolation network turns off or the active clamp network turns on thereby isolating sea of gates (12) from power rail (18, 20).